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MCF5200 PRM

Addendum to
MCF5200 Programmer's Reference Manual Rev 1.0

March 10, 1998
May 12, 1998

This addendum to the initial release of the MCF5200PRM/AD User's Manual (Rev 1.0) provides corrections to the original text, plus additional information not included in the original. This document and other information on this product is maintained on the World Wide Web at http://sps.motorola.com/coldfire.

Correction to Effective Addressing Modes and Categories

Page 2-13 of the Programmer's Reference Manual shows an incorrect Mode Field for Absolute Data Addressing, Long entry, Reg. Field. It should read "001", and not "000".

Table 2-3. Effective Addressing Modes and Categories

Addressing Modes	Syntax	Mode Field	Reg. Field	Data	Memory	Control	Alterable
Register Direct							
Data	Dn	000	reg. no.	X	—	—	X
Address	An	001	reg. no.	—	—	—	X
Register Indirect							
Address	(An)	010	reg. no.	X	X	X	X
Address with Postincrement	(An)+	011	reg. no.	X	X	—	X
Address with Predecrement	–(An)	100	reg. no.	X	X	—	X
Address with Displacement	(d_{16},An)	101	reg. no.	X	X	X	X
Address Register Indirect with Index 8-Bit Displacement	(d_8,An,Xn)	110	reg. no.	X	X	X	X
Program Counter Indirect with Displacement	(d_{16},PC)	111	010	X	X	X	—
Program Counter Indirect with Index 8-Bit Displacement	(d_8,PC,Xn)	111	011	X	X	X	—
Absolute Data Addressing							
Short	(xxx).W	111	000	X	X	X	—
Long	(xxx).L	111	001	X	X	X	—
Immediate	#<xxx>	111	100	X	X	—	—

Clarification of JSR (Jump to Subroutine) Instruction

Note that if the JSR target uses a 16-bit address, it is sign-extended.

CPUSHL entry

CPUSHL on page 5-3 has listed as arguments: “, <ea>, (Ax)”. This should read as only (Ax).

Missing Instruction Descriptions.

Pages 5-14 & 5-15 should have instruction description for WDDATA & PULSE instructions as follows:

WDDATA Write to Debug DataWDDATA

Operation: Source --> DDATA Signal Pins

Assembler Syntax : WDDATA <ea>

Attributes: Size = Byte, Word, Long Word
Description: This instruction fetches the operand defined by the effective address and captures the data in the ColdFire debug module for display on the DDATA output pins. The size of the operand determines the number of nibbles displayed on the DDATA output pins. The value of the debug module configuration/status register (CSR) does not affect the operation of this instruction.

The execution of this instruction generates a processor status encoding matching the PULSE instruction before the referenced operand is displayed on the DDATA outputs.

Condition Codes: Not affected

Instruction Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	0	0	SIZE		EFFECTIVE ADDRESS					
										MODE			REGISTER		

Instruction Fields:

Size field—specifies the size of the operand data:
00—byte operation
01—word operation
10—long operation

Effective Address field—determines the addressing mode for the operand to be written to the DDATA signal pins; use only those memory alterable addressing modes listed in the following table:

Addressing Mode	Mode	Register
Dn	—	—
An	—	—

Addressing Mode	Mode	Register
(xxx).W	111	000
(xxx).L	111	001

Addressing Mode	Mode	Register
(An)	010	reg. number: An
(An) +	011	reg. number: An
-(An)	101	reg. number: An
(d_{16}, An)	101	reg. number: An
(d_8, An, Xn)	110	reg. number: An

Addressing Mode	Mode	Register
#<data>	—	—
(d_{16}, PC)	—	—
(d_8, PC, Xn)	—	—

PULSEGenerate a Unique Processor StatusPULSE

Operation: Generate a Unique Processor Status Encoding

Assembler Syntax: PULSE

Attributes: Unsized

Description: This instruction does not perform any explicit operation except for the generation of a unique encoding of the processor status output pins (PST = $4). This encoding is asserted by one processor clock cycle and is useful in providing a trigger to external logic during debug, performance characterization, etc.

Condition Codes: Not affected

Instruction Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	0	1	0	1	1	0	0	1	1	0	0

Correction to Operation Code Maps

Page 6-9 of the Programmer's Reference Manual shows an incorrect Code Map for the PULSE instruction. The correct map is :

30. PULSE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	0	1	0	1	1	0	0	1	1	0	0

Page 6-13 of the Programmer's Reference Manual shows an incorrect Code Map for the WDDATA instruction. The correct map is :

66. WDDATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	0	0	SIZE		EFFECTIVE ADDRESS					
										MODE			REGISTER		

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